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PATENT
Attorney Docket No. 502370
Client Reference No. 96517US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Gregory T. Momber

Application No. 09/913,859

Filed: March 28, 2002

Art Unit: 2836

Examiner: Brett S. Squires

For: TRANSFORMERLESS POWER SUPPLY, DUAL POSITIVE OR DUAL NEGATIVE SUPPLIES

APPELLANT'S APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of the appeal from the final rejection dated February 9, 2005, Appellant now submits his Brief.

Real Party In Interest

The patent application that is the subject of this appeal is assigned to Robertshaw Controls Company.

Related Appeals and Interferences

We are not aware of any appeals or interferences that are related to this appeal.

Status of Claims

Claims 1, 3-13, and 15-25 are pending and stand finally rejected, and these rejections are presently being appealed. Claims 2 and 14 have been previously cancelled. A complete listing of the claims on appeal appears at Appendix A.

Status of Amendments

There are no outstanding amendments.

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Art Unit: 2836

Examiner: Brett S. Squires

TRANSMITTAL OF
APPELLANT'S APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 CFR 41.37, appellant hereby submits Appellant's Brief on Appeal.

The items checked below are appropriate:

1. Status of Appellants

This application is on behalf of ☒ other than a small entity or ☐ a small entity.

2. Fee for Filing Brief on Appeal

Pursuant to 37 CFR 41.20(2), the fee for filing the Brief on Appeal is for: ☒ other than a small entity or ☐ a small entity.

Brief Fee Due $500.00

3. Oral Hearing

☐ Appellants request an oral hearing in accordance with 37 CFR 41.47.
A separate paper requesting oral hearing is attached.

4. Extension of Time

☐ Appellants petition for a one-month extension of time under 37 CFR 1.136, the fee for which is $ 0.00.

☒ Appellants believe that no extension of time is required. However, this conditional petition is being made to provide for the possibility that

appellants have inadvertently overlooked the need for a petition and fee for extension of time.

Extension fee due with this request: $

5. **Total Fee Due**

The total fee due is:

Brief on Appeal Fee	$500.00
Request for Oral Hearing	$ 0.00
Extension Fee (if any)	$ 0.00

Total Fee Due: $500.00

6. **Fee Payment**

☐ Attached is a check in the sum of $.
☒ Charge Account No. 12-1216 the sum of $500.00. A duplicate of this transmittal is attached.

7. **Fee Deficiency**.

☒ If any additional fee is required in connection with this communication, charge Account No. 12-1216. A duplicate copy of this transmittal is attached.

Respectfully submitted,

Phillip M. Pippenger, Reg. No. 46,055
LEYDIG, VOIT & MAYER, LTD.
Two Prudential Plaza
180 North Stetson Ave., Suite 4900
Chicago, Illinois 60601-6780
(312) 616-5600 (telephone)
(312) 616-5700 (facsimile)

Date: June 28, 2005

CERTIFICATE OF MAILING

I hereby certify that this APPEAL BRIEF TRANSMITTAL AND APPEAL BRIEF (along with any documents referred to as attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date: June 28, 2005 Susan Matz

Summary of Claimed Subject Matter

There are 23 pending claims, of which claims 1, 13, 15, 22 and 23 are independent. The summaries hereinafter reference the replacement specification filed on November 9, 2004.

Independent claim 1 pertains to a dual output transformerless power supply (*See* Figs. 5(a)-5(d)) having (1) a first dc output stage (*See* Fig, 5(a), lower output of $-V_s$, and page 5, ll. 6-25) for receiving an ac input (*Id.*, L1 and N) and providing a dc output of a first polarity (*Id.*, -Vs), the stage including a wave rectifier with at least one diode (*Id.*, diode 23) and a voltage regulator with at least one zener diode (*Id.*, zener diodes 32, 33), and (2) a second dc output stage (*See* Fig, 5(a), upper output of $-V_s$, and page 5, ll. 6-25) for receiving an ac input (*Id.*, L1 and N) and providing a dc output of the same polarity as the first (*Id.*, -Vs), also having a wave rectifier including at least one diode (*Id.*, diode 20), with a regulated dc output (the node between diode 20 and capacitor 41) inverted by an inverter (*Id.*, transistor 50) connected to the wave rectifier (See page 4, l. 25 through page 5, l. 5), and also including a second voltage regulator containing at least one zener diode (*Id.*, zener diodes 30, 31).

Independent claim 13 pertains to a dual output transformerless power supply that includes a first means for rectifying an ac input to generate a first dc output signal having a first polarity (*See* Fig. 5(a), diode 23, and page 5, ll. 6-25) and a second means for rectifying the ac input to generating a second dc output signal (*Id.*, diode 20). Finally, the dual output transformerless power supply of claim 13 also includes means for inverting the second dc output signal to the first polarity. (*Id.*, transistor 50). The transistor 50 is configured as an inverter and in operation has the effect of inverting the second dc output, i.e. the voltage between diode 20 and capacitor 41.

Independent claim 15 pertains to a dual output transformerless power supply that includes a first means for rectifying an ac input to generate a first dc output signal having a first polarity (*See* Fig. 5(a), diode 23, and page 5, ll. 6-25) and a second means for rectifying the ac input to generating a second dc output signal (*Id.*, diode 20) of the same polarity. Finally, the dual output transformerless power supply of claim 15 also includes means (transformer 50) for shifting the ac input 180 degrees for input into the second means for rectifying.

Independent claim 22 pertains to a dual output transformerless power supply having (1) first means for rectifying an ac input generating a first dc output signal having a first polarity (*See* Fig. 5(a), diode 23, and page 5, ll. 6-25); (2) first means for filtering said first dc output signal connected to said first means for rectifying (*Id.*, capacitor 43); (3) first means for voltage

regulation connected to said means for filtering (*Id.*, zener diodes 32 and 33); (4) second means for rectifying an ac input generating a second dc output signal having said first polarity (*Id.*, diode 20, *see also* page 4, l. 25 through page 5, l. 5); (5) second means for filtering said second dc output signal connected to said second means for rectifying (*Id.*, capacitor 41, *see also* page 5, ll. 6-25); (6) second means for voltage regulation connected to said second means for filtering (*Id.*, zener diodes 30 and 31, *see also* page 4, l. 25 through page 5, l. 5); and (7) means for inverting connected to said second means for voltage regulation (*Id.*, transistor 50; *see* page 5, ll. 6-25).

Independent claim 23 pertains to a method for providing a dual output transformerless power supply comprising the steps of (1) converting an ac input signal during a first half-cycle to a first dc output with a first polarity, and (2) converting the ac input during a second half-cycle to a second dc output with the same polarity as the first dc output by inverting the second dc output. The specification describes the first half-cycle dynamics at paragraph 31 (page 4, l. 25 through page 5, l. 5). In particular, it is stated that "[o]n the positive-half cycle, diode (20) will conduct...voltage ... is developed across capacitor 41..." *Id.* The specification describes the second half-cycle dynamics at paragraph 32 (page 5, ll. 6-25) as follows: "During the negative-half cycle...voltage ...is developed across capacitor (43)...The transistor (50) will be turned on as soon as the line voltage goes negative and when this occurs, capacitor (41) is discharged into capacitor (42). This results in a voltage reversal at the anode of diode (21)."

Grounds of Rejection to be reviewed on Appeal

The grounds of rejection to be reviewed on appeal are those in the final Office Action of February 9, 2005. In that Action, all pending claims except claims 9 and 12 are rejected as anticipated by Pecore (US 6,014,325). Claim 9 is rejected as obvious over Pecore without further support, while claim 12 is rejected as obvious over Pecore in view of Tanoi (US 5,498,991). Accordingly, Applicant requests that the anticipation rejection as applied to each of the independent claims be reviewed on appeal.

The resolution of the first grounds of rejection will moot the rejections of dependent claims 9 and 12, since these dependent claims necessarily incorporate the limitations of their parent claims. However, Appellant will briefly address these rejections as well, and requests review thereof on appeal.

Argument

All pending claims recite or pertain to the use of an inverter in a dual output transformerless power supply. Although the independent claims stand rejected as anticipated

by Pecore, it goes without saying that an anticipation rejection is only proper when the cited reference teaches each element of the rejected claim. 35 USC § 102; *see also* MPEP § 2131. Where, as here, each claim contains one or more recitations for which there is no teaching in the cited reference, the rejections are unsustainable and must be reversed. In particular, each claim recites the use of an inverter (or 180 degree phase shifter), and this element is entirely absent from the teachings of Pecore.

<u>The Rejection of Claim 1 (and Claims 3-12)</u>

The Office action rejects claim 1 as anticipated by Pecore. Independent claim 1 and those claims dependent thereon require, inter alia, that the second dc output stage have a regulated dc output inverted by an inverter connected to the second wave rectifier. In this way, the dual output transformerless power supply provides either dual positive or dual negative outputs.

As discussed previously by the applicant during the prosecution of this application and as asserted by the Examiner, Fig. 2 of Pecore '325 shows two regulated dc outputs of the same polarity. However, neither this circuit nor any teaching of Pecore '325 includes or describes the use of an inverter connected to the second wave rectifier as required by this independent claim 1. The Examiner initially did not contradicted this point, but instead relied upon an unrelated definition of the term "inverter" from the IEEE Dictionary to state that the applicant's invention does not include an inverter. However, the Examiner selected a definition of the term "inverter" that is not consistent with the usage of that term in the present application, and that is clearly not the only way that this term is used in the art. When a term has several definitions, the Examiner must look to the intrinsic record of the specification and claims to see how a particular term is used therein.

In this case, the applicants have used the term "inverter" in accordance with its common usage in the art to identify a class of circuit elements that invert the polarity of a signal from its input to its output. For example, as described in paragraph [0010], this class of circuit elements may include a transistor in either the common emitter configuration or the common source configuration. Such a configured transistor is commonly known in the art as an inverter because it inverts the polarity of an applied signal. When this term is interpreted in view of the specification and in view of its common usage in the art, it is clear that the applicant's claimed invention does indeed include an inverter. The alternate definition of the term "inverter" as used in the electric power context as a machine, device, or system that

changes direct current power to alternating current power is clearly not applicable here. Thus, the Examiner's contention that "the applicant's transistor is not an inverter" is erroneous and should not be maintained. When the correct interpretation of the term "inverter" is applied, it is clear that Pecore does not anticipate this claim.

The Examiner has also argued that even if the transistor disclosed by the applicant is an inverter, the transistor of Pecore '325 illustrated in Fig. 2 as reference number 142 is also an inverter. However, this transistor does not invert the polarity of a signal connected to its input, but instead operates as a power switch to shut off the output voltage. Specifically, column 7, line 51 of Pecore '325 describes that the transistor is part of "a switching circuit 107 ... to short together terminals 116 and 113 of the 24 VDC stage in response to a control signal CS applied at terminal 115. By shorting these load terminals together, capacitor 132 cannot build up a potential sufficient to cause current to flow through zener diodes 134 and 136 .... This reduces the voltage across terminals 116 and 113 to a magnitude equal to the collector-emitter saturation voltage of voltage of transistor 142, or about 0.1 volts." This 0.1 volts is the same polarity as the output voltage across these terminals when the transistor is not turned on (24 VDC). Thus, this transistor 142 does not provide any inverting operation, and therefore cannot anticipate an inverter. Rather, Pecore's transistor is simply a power switch in the switching circuit "to reduce power consumption to near zero." Pecore '325, column 8, lines 15-16, 19-20. Nowhere in Pecore '325 is this transistor described as providing any inversion of the polarity of a signal.

In the Advisory Action dated June 17, 2005, the Examiner seems to admit the absence in Pecore of a separate inverter as such, and raises the new argument that the rectification diodes of Pecore themselves act as both rectifiers and inverter. But even if this were true, the claim at issue does not broadly recite rectifiers and inverters regardless of their relationship. Rather, claim 1 states "...a regulated dc output inverted by an inverter... ." Under the Examiner's reasoning in the June 17 Advisory Action, the "inverter" would be acting directly upon the ac input, not the recited regulated dc output.

Moreover, the diode configuration cited in Pecore is simply not an inverter configuration. Rather, the upper section of the circuit shown in Figure 2 passes current when source 112 is polarized in one direction, and the lower portion of the circuit passes current when the source is polarized in the other direction. Both sections pass positive voltage through and the outputs remain positive. Similarly, see, for example, the circuit of Figure 4. Here, diode 326 passes current when the source is polarized in one direction, whereas diode 327, connected at the same point, passes current when the source is polarized in the opposite direction. The net result

is that the outputs have different polarities. But again, neither diode acts as an inverter—each passes its input without changing the polarity thereof.

The sections of Pecore cited by the Examiner confirm, in fact, that the circuit elements in question rectify and do not invert. See, for example, column 7, ll. 4-6: "Thus, each pair of diodes 124, 126 and 128, 130 provides ***bi-directional half-wave rectification*** of the signal from the AC voltage source 112, each half wave therefore providing power to a separate stage of the supply."

In view of the above, the Appellant respectfully submits that claim 1 and claims 3-12, which depend from claim 1, are not anticipated by Pecore.

The Rejection of Claim 13 (and Claims 16-21)

Further, independent claim 13 requires a means for inverting the second dc output signal to be the first polarity. As discussed above, Pecore '325 does not include any means for inverting the second dc output signal to be the first polarity. Therefore, Pecore '325 also cannot anticipate claims 13 and 16-21 dependent thereon.

The Rejection of Claim 15

Independent claim 15 requires means for shifting an input signal 180 degrees. With regard to claim 15, the Examiner has again looked to an unrelated dictionary definition of the term "phase shift" to state that the applicant's invention does not provide for phase shifting as defined by the Examiner. However, as described by the present specification in paragraph [0029], during the negative-half cycle of the ac input signal, a transistor in either a common emitter or common source configuration may be used to shift the input signal by 180 degrees. Thus, the applicant's invention as claimed in claim 15 does indeed include phase shifting of the input signal by 180 degrees. Since the system of Pecore '325 does not include any such phase shifting by 180 degrees, it cannot anticipate this claim.

The Rejection of Claim 22

Similarly, independent claim 22 includes a recitation of "means for inverting" a specified signal. Since, as discussed above, the teachings of Pecore do not include any means for inverting any signal, Pecore cannot anticipate this claim.

The Rejection of Claim 23 (and Claims 24-25)

Independent claim 23 includes the step of converting a signal by inverting it. Again, since Pecore does not include an inverter, it cannot anticipate claim 23 or dependent claims 24-25.

The Rejection of Claim 9

Claim 9 depends from claim 1, and additionally recites that each of the first and second voltage regulator circuits comprises first and second zener diode in series. The Final Action rejects claim 9 as obvious, citing the existence of two zener diodes in series in one circuit of Pecore, and indicating that it would be obvious to use the same arrangement in the other circuit of Pecore.

However, there is no support for this assertion. The Action's only basis for modifying Pecore in this way is that "...mere duplication of the essential working parts of a device involves only routine skill in the art." It is not really clear what that means, but what is clear is that there is no prima facie case of obviousness here. It is *undisputed* that the Pecore reference in fact does *not* use two zener diodes in the circuit segment in question; presumably there was a reason for that arrangement. Given that background, why would one of skill in the art have been motivated to modify the reference to better match applicant's claims? No reason is given. If one of skill in the art had been ***told*** to modify the Pecore device, then maybe they could have, in line with the Examiner's statement regarding routine skill, or maybe they couldn't have– but as the rejection now stands, the question of ***why*** one would modify the reference's teachings remains unanswered.

The Rejection of Claim 12

Claim 12 depends indirectly from claim 1, and additionally recites that a relay voltage is controlled by a microprocessor which is controlled by a level shifter ciruit. The Final Action rejects claim 12 as obvious over Pecore in view of Tanoi. The Action's position appears to be that Pecore supplies all of the limitations except the level shifter, and Tanoi supplies the level shifter. According to the Action, it would be obvious to combine the references to "reduce the risk of the microprocessor being damaged by extremely high voltage signals and not being able to interpret extremely low voltage signals.

However, to the best of Appellant's knowledge, there is no indication in ***any*** of the art that the circuit of Pecore actually suffers from the listed "problems." Thus, the Examiner is "solving" a problem that the prior art doesn't have, solely to better match the art to Appellant's

claims. This is nothing more than hindsight, and is of course not a valid motivation for combining references.

Conclusion

All pending claims recite or pertain to the use of an inverter (or 180 degree phase shifter) in a dual output transformerless power supply. The applied reference, Pecore, does not teach the use of such an inverter or phase shifter. The Examiner's assertions have been carefully studied and considered, but the assertion that Pecore teaches such an inverter or phase shifter is simply erroneous from a factual and technical standpoint.

Accordingly, the claims on appeal cannot be anticipated by Pecore, and it is requested that the Examiner be instructed to withdraw the pending rejections.

Respectfully submitted,

Phillip M. Pippenger, Reg. No. 46,055
LEYDIG, VOIT & MAYER, LTD.
Two Prudential Plaza
180 North Stetson Ave., Suite 4900
Chicago, Illinois 60601-6780
(312) 616-5600 (telephone)
(312) 616-5700 (facsimile)

Date: June 28, 2005

Claims Appendix

1. (Previously Presented) A dual output transformerless power supply comprising:

a first dc output stage responsive to an ac input, having a first wave rectifier including at least one diode with a regulated dc output exhibiting a first polarity, and including a first voltage regulator having at least one zener diode; and

a second dc output stage responsive to said ac input, having a second wave rectifier including at least one diode with a regulated dc output inverted by an inverter connected to said second wave rectifier to be said first polarity, and including second voltage regulator having at least one zener diode.

3. (Previously Presented) A dual output transformerless power supply, according to claim 1, wherein said inverter includes a transistor connected to said second wave rectifier.

4. (Previously Presented) A dual output transformerless power supply, according to claim 1, wherein said inverter includes a transistor in a common emitter configuration connected to said second wave rectifier.

5. (Previously Presented) A dual output transformerless power supply, according to claim 1, wherein said inverter includes a transistor in a common source configuration connected to said second wave rectifier.

6. (Original) A dual output transformerless power supply, according to claim 1, further comprising:

a first capacitor connected to said first dc output stage; and a second capacitor connected to said second dc output stage.

7. (Original) A dual output transformerless power supply, according to claim 1, wherein:
said first voltage regulator circuit is connected to said first wave rectifier; and
said second voltage regulator circuit is connected to said second wave rectifier.

8. (Original) A dual output transformerless power supply, according to claim 1, further comprising:

said first voltage regulator circuit connected to said first wave rectifier having one or more zener diodes in series connected to a first filter; and

said second voltage regulator circuit connected to said second wave rectifier having one or more zener diodes in series connected to a second filter.

9. (Original) A dual output transformerless power supply, according to claim 1, further comprising:

said first voltage regulator circuit connected to said first wave rectifier having a first and second zener diode in series; and

said second voltage regulator circuit connected to said second wave rectifier circuit having a first and second zener diode in series.

10. (Original) A dual output transformerless power supply, according to claim 1, further comprising:

a first capacitor connected to the output of said first wave rectifier; and

a second capacitor connected to the output of said second wave rectifier.

11. (Original) A dual output transformerless power supply, according to claim 1, further comprising:
a relay voltage which is controlled by a microprocessor.

12. (Original) A dual output transformerless power supply, according to claim 11, wherein the microprocessor is controlled by a level shifter ciruit.

13. (Previously Presented) A dual output transformerless power supply comprising:

first means for rectifying an ac input generating a first dc output signal having a first polarity;

second means for rectifying an ac input generating a second dc output signal; and

means for inverting said second dc output signal to be said first polarity.

15. (Previously Presented) A dual output transformerless power supply comprising:

first means for rectifying an ac input generating a first dc output signal having a first polarity;

second means for rectifying an ac input generating a second dc output signal having said first polarity; and

means for shifting said ac input 180 degrees for input into said second means for rectifying.

16. (Original) A dual output transformerless power supply, according to claim 13, further comprising:

first means for filtering said first dc output signal.

17. (Original) A dual output transformerless power supply, according to claim 13, further comprising:

second means for filtering said second dc output signal.

18. (Original) A dual output transformerless power supply, according to claim 16, further comprising:

second means for filtering said second dc output signal.

19. (Original) A dual output transformerless power supply, according to claim 13, further comprising:

first means for voltage regulation of said first dc output signal.

20. (Original) A dual output transformerless power supply, according to claim 13, comprising:

second means for voltage regulation of said second dc output signal.

21. (Original) A dual output transformerless power supply, according to claim 19, further comprising:

second means for voltage regulation of said second dc output signal.

22. (Original) A dual output transformerless power supply comprising:

first means for rectifying an ac input generating a first dc output signal having a first polarity;

first means for filtering said first dc output signal connected to said first means for rectifying;

first means for voltage regulation connected to said means for filtering;

second means for rectifying an ac input generating a second dc output signal having said first polarity;

second means for filtering said second dc output signal connected to said second means for rectifying;

second means for voltage regulation connected to said second means for filtering;

means for inverting connected to said second means for voltage regulation.

23. (Previously Presented) A method for providing a dual output transformerless power supply comprising the steps of:

converting an ac input signal during a first half-cycle to a first dc output with a first polarity;

converting the ac input during a second half-cycle to a second dc output with the same polarity as the first dc output by inverting the second dc output.

24. (Original) A method for providing a dual output transformerless power supply, according to claim 23, further comprising the step of:

providing a relay voltage.

25. (Original) A method for providing a dual output transformerless power supply, according to claim 24, further comprising the step of:

controlling the relay voltage with a control circuit.